What is claimed is:

1. A parallel processor for processing a plurality of operation instructions in one cycle in parallel, comprising:

a first operation processor; and

at least one second operation processor,

the first operation processor including,

an operation mode retaining unit for retaining an operation mode indicating whether or not the second operation processor should be run in parallel to carry out an operation instruction, wherein the operation mode has a first operation mode in which the first operation processor alone is operated, and a second operation mode in which both of the first operation processor and the second operation processor are operated,

a control unit for, in case that the operation mode is the first operation mode, in accordance with the operation mode, supplying the first operation processor with an instruction sequence that defines an operation of the first operation processor, and for generating a control signal to halt an operation of the second operation processor and supplying the control signal to the second operation processor, whereby as to an instruction of the first operation mode, the second operation processor is not operated without embedding an instruction that defines an operation of the second operation processor in the instruction sequence retained in an instruction memory, and

an instruction execution unit for switching the operation mode in accordance with an input decoded instruction.

2. The parallel processor according to claim 1, wherein:

when the operation mode is the second operation mode, the control unit supplies the first operation processor with an instruction string that defines an operation of the first operation processor, and supplies the second operation processor with an instruction string that defines an operation of the second operation processor.

3. The parallel processor according to claim 1, wherein: the control signal is a no operation instruction.

4. The parallel processor according to claim 1, wherein: in the first operation mode, the instruction sequence retained in the instruction memory includes only an instruction that defines an operation of the first operation processor.

5. The parallel processor according to claim 3, wherein:

the control unit includes a no operation instruction retaining unit for retaining the no operation instruction; and

in the first operation mode, the instruction string retained in the instruction memory constantly includes a plurality of instructions.

6. The parallel processor according to claim 1, wherein:

the control signal is a signal that stops a supply of a clock to the second operation processor.

7. The parallel processor according to claim 1, wherein:

the control signal is a disable signal of the second operation processor.

8. The parallel processor according to claim 1, wherein:

the instruction execution unit switches the operation mode retained in the operation mode retaining unit by executing a sub-routine call instruction directing an operation mode switching.

9. The parallel processor according to claim 8, wherein:

the operation mode retaining unit is an operation mode register;

the control unit includes a first return address register for retaining a return address from the sub-routine call instruction;

the instruction execution unit, when executing the sub-routine call instruction, switches the operation mode by inverting a value in the operation mode register, and sets information indicating inversion of the operation mode in the first return address register, and

when returning from the sub-routine call instruction, refers to the information indicating the inversion of the operation mode set in the first return address register, and if the inversion is set, returns to the operation mode set before the sub-routine call instruction by inverting the value in the operation mode register.

10. The parallel processor according to claim 1, wherein:

the instruction execution unit switches the operation mode retained in the operation mode retaining unit at an occurrence of an exception.

11. The parallel processor according to claim 10, wherein:

the operation mode retaining unit is an operation mode register;

the control unit includes a second return address register for retaining a return address from an exception handling program by which the exception handling is carried out;

the instruction execution unit, at an occurrence of the exception, switches the operation mode by inverting the value in the operation mode register, and sets information indicating inversion of the operation mode in the second return address register, and

when returning from the exception, refers to the information indicating the inversion of the operation mode set in the second return address register, and if the inversion is set, returns to the operation mode set before the exception by inverting the value in the operation mode register.

12. The parallel processor according to claim 1, wherein:

the instruction execution unit switches the operation

mode by inverting the value in the operation mode retaining unit in accordance with information indicating inversion of the operation mode contained in a part of a jump address defined in a jump instruction.

13. The parallel processor according to claim 1, wherein:

the second operation processor comprises a plurality of coprocessors; and

the control unit, in the first operation mode, operates the first operation processor alone by stopping clocks to the plurality of coprocessors other than the first operation processor.

14. The parallel processor according to claim 1, further comprising:

an extended operation mode retaining unit for retaining an extended operation mode indicating which of the plurality of second operation processors should be operated to carry out the operation instruction in parallel,

wherein,

the control unit supplies the control signal to, in accordance with the extended operation mode, the second operation processor other than the second operation processor which is indicated by the extended operation mode.

15. A computer system equipped with a parallel processor for processing more than one operation instruction in one cycle, comprising:

a first operation processor;

at least one second operation processor; and

a data memory,

the first operation processor including,

an operation mode retaining unit for retaining an operation mode indicating whether or not the second operation processor should be run in parallel to carry out an operation instruction, wherein the operation mode has a first mode in which

the first operation processor alone is operated, and a second operation mode in which both of the first operation processor and the second operation processor are operated,

a control unit for, in case that the operation mode is the first operation mode, in accordance with the operation mode, supplying the first operation processor with an instruction sequence that defines an operation of the first operation processor, and for generating a control signal to halt an operation of the second operation processor and supplying the control signal to the second operation processor, whereby as to an instruction of the first operation mode, the second operation processor is not operated without embedding an instruction that defines an operation of the second operation processor in the instruction sequence retained in an instruction memory, and

an instruction execution unit for switching the operation mode in accordance with an input decoded instruction.

16. The computer system according to claim 15, wherein:

when the operation mode is the second operation mode, the control unit supplies the first operation processor with an instruction string that defines an operation of the first operation processor, and supplies the second operation processor with an instruction string that defines an operation of the second operation processor.

17. The computer system according to claim 15, wherein:
the control signal is a no operation instruction.

18. The computer system according to claim 15, wherein:
in the first operation mode, the instruction string retained in the instruction memory includes only an instruction that defines an operation of the first operation processor.

19. The computer system according to claim 17, wherein:
the control unit includes a no operation instruction

retaining unit for retaining the no operation instruction; and

in the first operation mode, the instruction string retained in the instruction memory constantly includes a plurality of instructions.

20. The computer system according to claim 15, further comprising:

an extended operation mode retaining unit for retaining an extended operation mode indicating which of the plurality of second operation processors should be operated to carry out an operation instruction in parallel,

wherein,

the control unit supplies the control signal to, in accordance with the extended operation mode, the second operation processor other than the second operation processor which is indicated by the extended operation mode, and

the control signal is a signal that stops a supply of a clock to the second operation processor.